

UNICAST/MULTICAST SYSTEM

FIELD OF THE INVENTION

This invention relates to a system for unicasting or
5 multicasting IP packets, ATM cells etc.

BACKGROUND OF THE INVENTION

As a switch for processing a multicast cell, for example,
Japanese patent application laid-open No.9-162879 (1997) discloses
a shared buffer type ATM. This ATM switch has address buffers
provided for its output ports, respectively. The multicast is
conducted by sequentially transferring the address pointer of a
shared buffer where a multicast cell is stored. Also, the ATM switch
needs to be provided with a counter for confirmation of the number
of broadcast to be decremented every time a multicast cell is output.

However, the ATM switch has problems below.

The first problem is that it is necessary to provide a large
amount of the buffer for multicast so as to cope with a case that
the ratio of multicast cells in traffic increases.

The second problem is that it may cause the lowering of
throughput since the subsequent multicast processing cannot be run
before the counter for confirmation of the number of broadcast
becomes zero.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the invention to provide a
unicast/multicast system that allows a unicast cell and a multicast
cell to be processed in the same circuit.

According to the invention, a unicast/multicast system,

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comprises:

an internal cell generating section that generates an internal cell based on user data;

5 an internal cell receiving section that outputs the internal cell to a timing generating section and outputs a header field of the internal cell to an index search section;

an output port conversion table that stores the relation of output index information and output port number in the form of one-to-one for the unicast and one-to-multiple for the multicast;

10 the index search section that extracts output index information from the header field to be sent from the internal cell receiving section, refers to the output port conversion table for an output port number corresponding to the output index information extracted, and outputs the output port number obtained from the output port conversion table to a destination-based distribution section;

15 the destination-based distribution sections that controls a gate section based on the output port number input from the index search section;

20 a timing generating section that delays the internal cell input from the internal cell receiving section and then outputs it the gate section;

the gate section that distributes the internal cell input from the timing generating section to the gate section according to the control of the destination-based distribution section;

25 a plurality of buffers that each store the internal cell distributed from the gate section and, when receiving the internal cell distributed from the gate section, sends switching request signal to a switching request adjusting section;

the switching request adjusting section that adjusts the

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switching request signal input from the buffers between the buffers and determines a route in a crosspoint switch; and

the crosspoint switch that outputs the internal cell stored in the buffers through the route determined by the switching request
5 adjusting section.

~~According to another aspect of the invention,~~

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be explained in more detail in conjunction with the appended drawings, wherein:

10 FIG.1 is a block diagram showing the schematic composition of a unicast/multicast system in a preferred embodiment according to the invention;

FIG.2 is a flow chart showing the operation of the unicast/multicast system in FIG.1;

15 FIG.3 is a format diagram showing an internal cell used in the unicast/multicast system in the embodiment of the invention;

FIG.4 is a block diagram showing the composition of a unicast/multicast system in a first preferred embodiment according to the invention;

20 FIG.5 is a table showing the content of a memory 13B in FIG.4;

FIG.6 is a block diagram showing the composition of a unicast/multicast system in a second preferred embodiment according to the invention; and

25 FIG.7 is a format diagram showing an internal cell used in the unicast/multicast system in FIG.6.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The preferred embodiments of the invention will be explained below, referring to the drawings.

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FIG.1 is a block diagram showing the schematic composition of a unicast/multicast system according to the invention. In FIG.1, 10 is an internal cell generating section to generate a cell (hereinafter referred to internal cell) with a fixed length and a specific format dedicated to switching, based on user data such as IP packet (Internet protocol), ATM (asynchronous transfer mode) cell etc. 11 is an internal cell receiving section that has a function to extract a header field from the internal cell. 12 is an index search section to get output port information corresponding to output index information included in the header field by referring to an output port conversion table 13. 13 is the table to store multiple index information and multiple output port number information in the form of one-to-one for the unicast and one-to-multiple for the multicast. 14 is a timing generating section to make the output of internal cell delay a predetermined time. 15 is a gate section that functions as a route to buffers 17-1 to 17-n to store the internal cell. 16 is a destination-based distribution section that controls the gate section 15 according to the output port information. 17-1 to 17-n are the FIFO (first-in first-out) type buffers that are provided for output ports, respectively, and store the internal cell for corresponding one of the output ports. Optionally, the buffers 17-1 to 17-n may be divided into buffers for the unicast and buffers for the multicast. 19 is a switching request adjusting section that controls a crosspoint switch 20 according to a switching request from the buffers 17-1 to 17-n.

Referring to FIGS.1, 2 and 3, the operation of the unicast/multicast system explained above will be explained below.

The internal cell generating section 10 converts global user data such as IP packet and ATM cell into internal cell. As shown

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by a format diagram in FIG. 3, an internal cell 40 is composed of a header field 41 and a data field 42. The header field 41 stores destination information such as VPI/VCI (virtual path identifier/virtual channel identifier) etc. that is converted into particular and simple form so that the internal cell is correctly subject to the switching inside the unit. The data field 42 stores the original user data. The internal cell receiving section 11 receives the internal cell 40 (step S11). Then, the internal cell receiving section 11 sends the header field 41 of the received internal cell 40 to the index search section 12, and sends the entire internal cell 40 to the timing generating section 14 (step S12). The index search section 12 extracts output index information from the header information of the header field 41 (step S15). After extracting the output index information of the header field 41, the index search section 12 gets output port number by referring to the output port conversion table 13 (step S16). The index search section 12 sends the obtained output port number to the destination-based distribution section 16. The destination-based distribution section 16 controls the gate section 15 according to the output port number received from the index search section 12 (step S17). In this case, when only one output port number is obtained, the gate to one output port opens, and when multiple output port numbers are obtained, the gates to multiple output ports open. On the other hand, the timing generating section 14 makes the internal cell sent to the timing generating section 14 delay the predetermined time that is necessary for the index search section 12 to search the output port number and for the destination-based distribution section 16 to control the gate section 15 (step S13). After the route of gate section 15 is determined, the internal cell is stored, through the

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gate section 15, into a specific buffer 17-i ($1 \leq i \leq n$) corresponding to the output port in case of the unicast, and into multiple buffers 17- i_1 , ..., 17- i_m ($i_1 \geq 1$ and $i_m \leq n$) in case of the multicast (step S14, S18). After the internal cell is stored in the buffer 17-i or buffers 17- i_1 , ..., 17- i_m , the buffer 17-i or buffers 17- i_1 , ..., 17- i_m sends the switching request to the switching request adjusting section 19 (step S19). The switching request adjusting section 19 conducts fairly the adjustment to the switching request received from the multiple buffers 17-1 to 17-n in a unit time, and determines the route of the crosspoint switch 20 (step S20). The crosspoint switch 20 establishes the route to pass the internal cell based on the route information from the switching request adjusting section 19, and conducts the switching of the internal cell (step S21).

[First Embodiment]

A unicast/multicast system in the first preferred embodiment according to the invention will be explained below, referring to FIGS. 4 and 5.

In this embodiment, as the output port conversion table 13, a memory 13B such as RAM (random access memory) or ROM (read-only memory) is used. In this case, the output index information to be extracted by a memory reading control circuit 12B to function as the index search section 12 corresponds to an address of the memory 13B, and the output port number corresponds to data to be written in each address of the memory 13B. Also, the memory 13B also functions as the destination-based distribution section 16. The output port number is stored in the form of bit pattern so as to facilitate the control of the gate section 15B. In case of the bit pattern form, the number n of ports corresponds to the data width of the memory 13B. Therefore, when a complete unicast region is, in advance, made

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using a memory of wide data width, it can cope with even such a case that the number n of ports increases, by adding bit pattern information for the multicast to the memory 13B.

FIG.5 shows an example of the content of the memory 13B in a case that there are 4095 ($=2^{12}-1$) types of output index information and there are 16 output ports. According to need, the output index information can be expanded to 65535 ($=2^{16}-1$) types. The address range of 000H to 00FH is used for the unicast, and the address range of 010H to FFFH is used for the multicast. In this way, bit patterns of "1" for only one bit are used for the unicast, and bit patterns of "1" for multiple bits are used for the multicast. Therefore, by using the composition and operation for the multicast, the unicast can be also handled.

When the memory reading control circuit 12B receives a header field from the internal cell receiving section 10, it extracts the output index information from the header field and then conducts the read operation to the memory 13B using the extracted output index information as address. In reply to this, the memory 13B outputs, as output port number, data corresponding to the output index information (=memory address). The gate section 15B allows a buffer corresponding to a bit with "1" of the data output from the memory 13B to be enabled.

On the other hand, an internal cell sent to a delay circuit 14B is delayed in the delay circuit 14B during the processing time required to determine the route of the gate section 15B. After the internal route of the gate section 15B is determined, the internal cell is output from the delay circuit 14, passing through the enabled buffer of the gate section 15B, written into only a FIFO type buffer corresponding to the enabled buffer. In case of the multicast, they

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are written into multiple FIFO buffers of the FIFO buffers 17-1 to 17-n, and in case of the unicast, it is written into one FIFO buffer of the FIFO buffers 17-1 to 17-n.

[Second Embodiment]

5 In the second preferred embodiment of the invention, even in a case that a multicast cell is desired to be subject to the priority switching, it is not necessary to provide separate circuits for the unicast and multicast in an existing circuit composition.

Referring to FIGS.6 and 7, the second embodiment will be explained below.

10 FIFO buffers 17C-1 to 17C-n are provided for output ports, respectively, and FIFO buffers 17D-1 to 17D-n are provided for output ports, respectively. The FIFO buffers 17C-1 to 17C-n are provided for the unicast, and the FIFO buffers 17D-1 to 17D-n are provided for the multicast. Also, a FIFO buffer 17C-i and a FIFO buffer 17D-i are provided for an i-th output port. The gate section 15B is the same as that in the first embodiment. A gate section 15C in the second embodiment is an additional gate, and allows an internal cell passed through the gate section 15B to be alternatively supplied to either
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20 FIFO 17C-i for the unicast or FIFO 17D-i for the multicast. The internal cell receiving section 10, memory 13B and delay circuit 14 are the same as those in the first embodiment.

FIG.7 shows the format of internal cell used in the second embodiment. In FIG.7, an internal cell 40 used in the second
25 embodiment is provided with a unicast/multicast identifier 71 and output index information 72 in header field 41. Similarly to the first embodiment, global user data such as IP packet and ATM cell are stored in data field 73.

When the internal cell receiving section 10 receives an internal

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cell, it extracts the header field of the internal cell and sends it to the memory reading control circuit 12C. Then, the memory reading control circuit 12C outputs the unicast/multicast identifier 71 of the header field to the gate section 15C, and outputs the output index information 72 thereof to the memory 13B. The memory 13B outputs, similarly to the first embodiment, a bit pattern corresponding to the output index information. The gate section 15B allows, similarly to the first embodiment, a buffer corresponding to a bit with "1" of the output bit pattern to be enabled. The gate section 15C allows a buffer corresponding to a FIFO buffer 17C-i for the unicast or a FIFO buffer 17D-i for the multicast to be enabled, according to the value of the unicast/multicast identifier 71. On the other hand, like the first embodiment, the internal cell sent from the internal cell receiving section 10 to the delay circuit 14B is delayed in the delay circuit 14B during a predetermined time, then passed through the enabled buffer of the gate section 15B. Then, if the unicast is designated by the unicast/multicast identifier 71, the internal cell passed through the enabled buffer of the gate section 15B is passed through a buffer of the gate section 15C corresponding to a FIFO buffer 17C-i for the unicast and written into the FIFO buffer 17C-i for the unicast. If the multicast is designated by the unicast/multicast identifier 71, the internal cell is passed through buffers of the gate section 15C corresponding to FIFO buffers 17D-i for the multicast and written into the FIFO buffers 17D-i for the multicast. Buffer management sections 17E-1 to 17E-n monitor the existence of internal cell stored in the FIFO buffers 17C-1 to 17C-n and 17D-1 to 17D-n. When it detects that the internal cell is stored in any of the FIFO buffers, it sends the switching request to the switching request adjusting section 19. When the transfer

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allowance to the crosspoint switch is issued from the switching request adjusting section 19, if there is stored a multicast cell, the buffer management sections 17E-1 to 17E-n transfers, by priority, the multicast cell to the crosspoint switch.

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Advantages of the invention:

First, since a unicast cell is similarly handled in the particular form of multicast cell, separate circuits for unicast cell and multicast cell is not necessary. Therefore, the processing circuit can be simplified.

Second, although the conventional system needs to be provided with separate buffers for the storing inside the system since the unicast cell and multicast cell are processed therein separately, in this invention the buffers for the multicast are not needed since the multicast cell is processed like the unicast cell.

Third, even when it is used with a crosspoint switch having no multicast function (=being not able to connect simultaneously to multiple routes), the multicast can be achieved.

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Although the invention has been described with respect to specific embodiment for complete and clear disclosure, the appended claims are not to be thus limited but are to be construed as embodying all modification and alternative constructions that may be occurred to one skilled in the art which fairly fall within the basic teaching here is set forth.

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